

ABSTRACT

5 A low power, high speed full adder cell is described. This cell
supports all possible combinations of active high/active low input/output
signal polarity (32 different combinations), without adding extra
inverters or extra transistors. The cell makes liberal use of CMOS
transmission gates in order to minimize the number of transistors used,
and to minimize their stacking. This significantly decreases the total
transistor gate area consumed, resulting in minimal power dissipation
10 and minimal cell size.